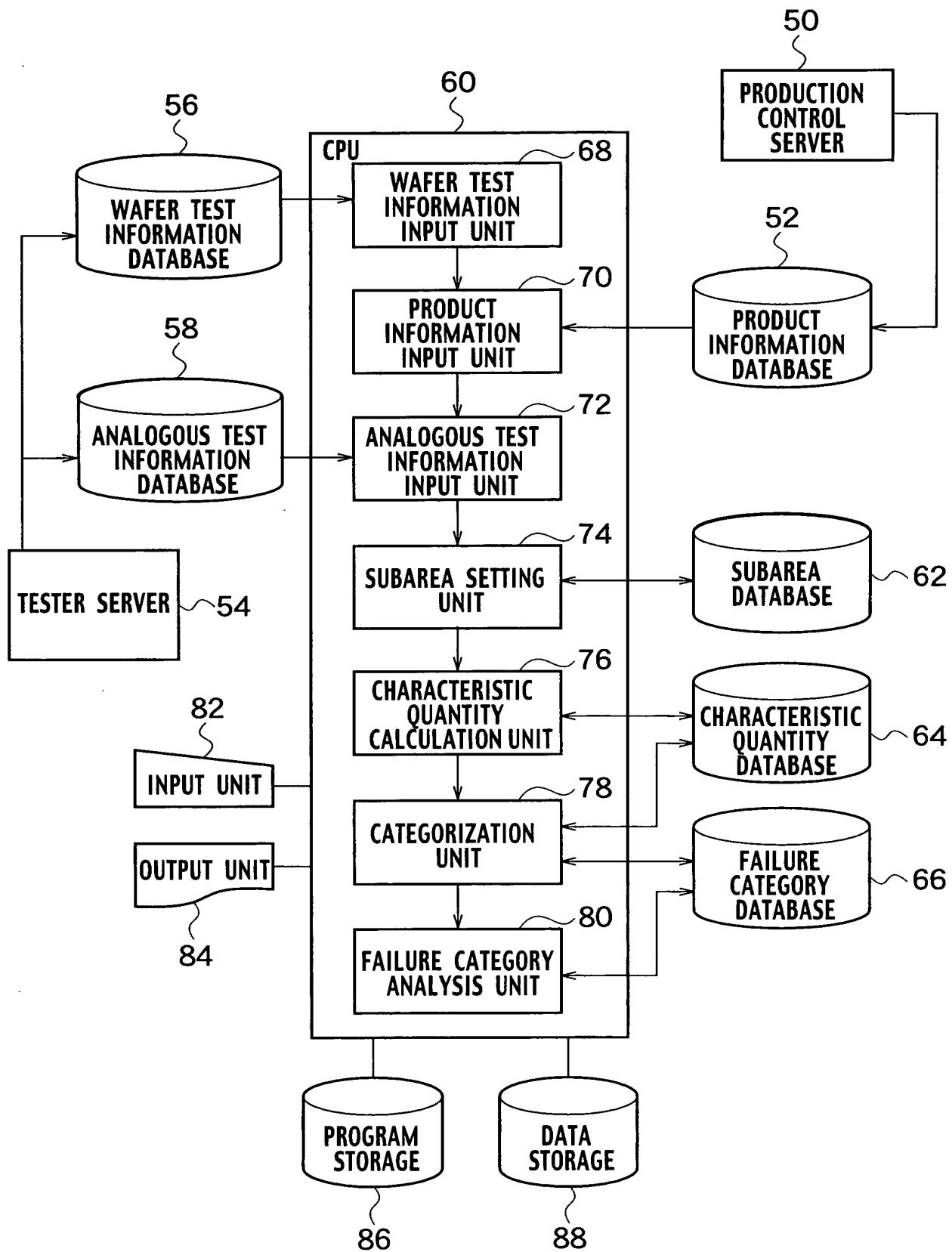
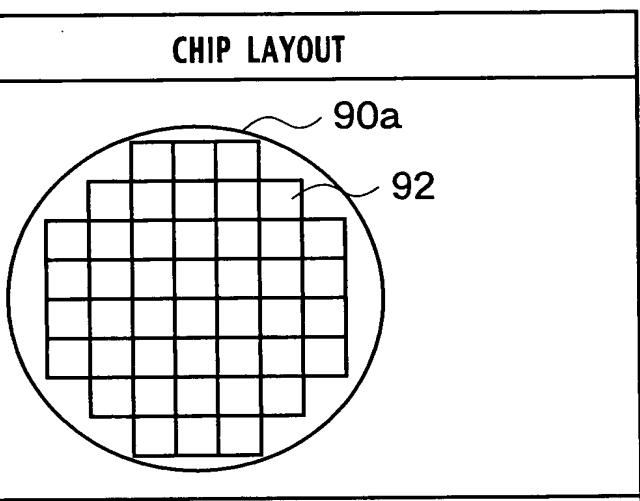
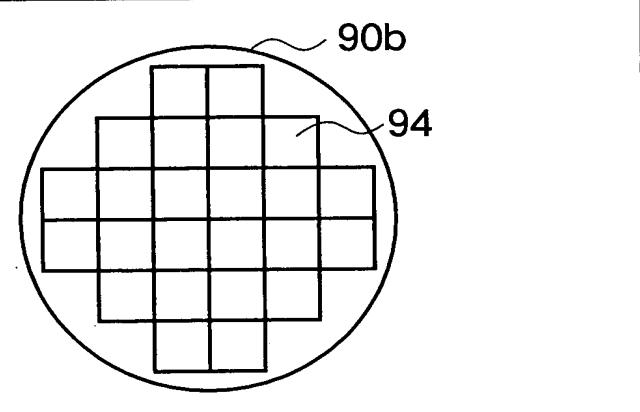
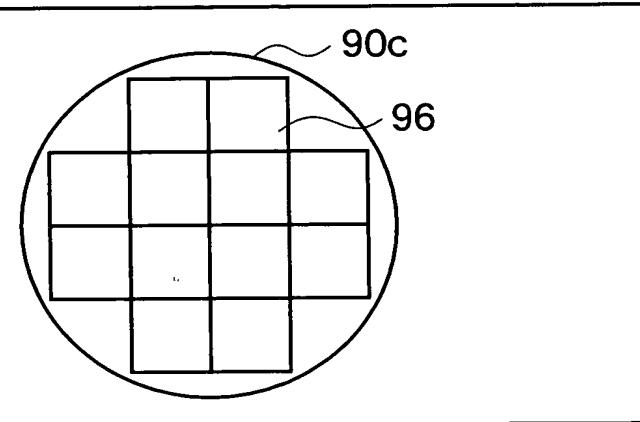


FIG. 1



**FIG. 2**

PRODUCT NAME	PRODUCT	CHIP LAYOUT
PRODUCT A	MEMORY	 90a 92
PRODUCT B	LOGIC	 90b 94
PRODUCT C	MEMORY MERGED LOGIC	 90c 96

**FIG. 3**

PRODUCT A		PRODUCT B		PRODUCT C	
ELECTRIC TEST	FAILURE CODE	ELECTRIC TEST	FAILURE CODE	ELECTRIC TEST	FAILURE CODE
DC	DC	POWER SHORT	PS	DC	DC
FUNCTION	FC	FUNCTION	FC	AD / DA1	A1
MARGIN	MA	FREQUENCY	FQ	AD / DA2	A2
		OTHER LOGIC	OL		

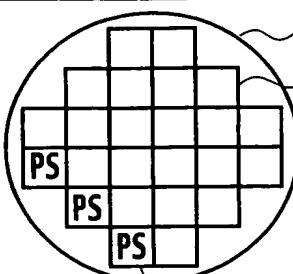
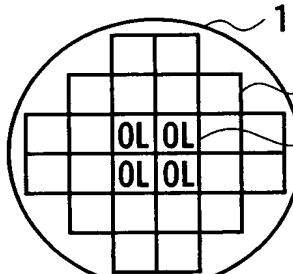
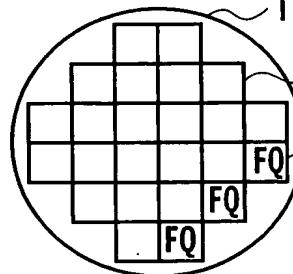
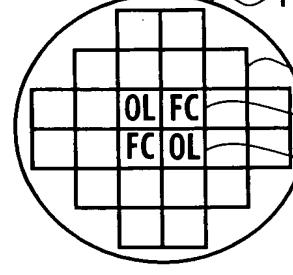
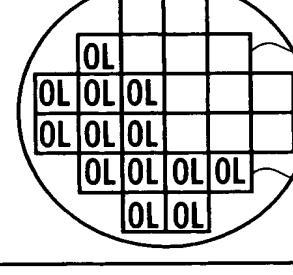
FIG. 4

ANALOGOUS ELECTRIC TEST 1			ANALOGOUS ELECTRIC TEST 2			ANALOGOUS ELECTRIC TEST 3		
PRODUCT	ELECTRIC TEST	FAILURE CODE	PRODUCT	ELECTRIC TEST	FAILURE CODE	PRODUCT	ELECTRIC TEST	FAILURE CODE
PRODUCT A	DC	DC	PRODUCT A	FUNCTION	FC	PRODUCT A	MARGIN	MA
PRODUCT B	POWER SHORT	PS	PRODUCT B	FUNCTION	FC	PRODUCT B	FREQUENCY	FQ
PRODUCT C	DC	DC	PRODUCT C	OTHER LOGIC	0L	PRODUCT C	AD / DA2	A2
			PRODUCT D	AD / DA1	A1			

FIG. 5

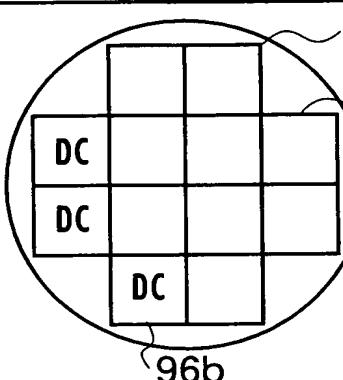
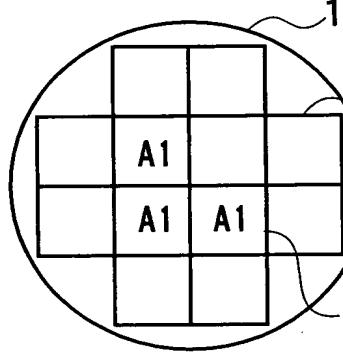
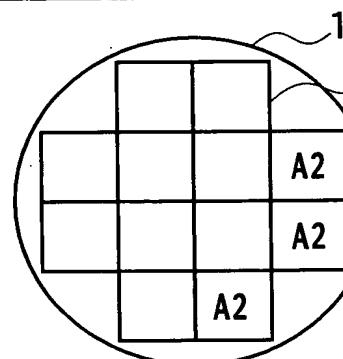
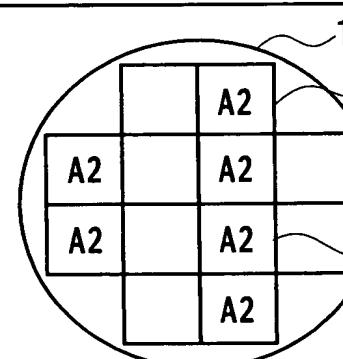
PRODUCT A WAFER NUMBER	ELECTRIC TEST RESULT
1	<p>100a</p> <p>92a</p> <p>92b</p>
2	<p>100b</p> <p>92a</p> <p>92c</p>
3	<p>100c</p> <p>92a</p> <p>92d</p>
4	<p>100d</p> <p>92b</p> <p>92a</p>

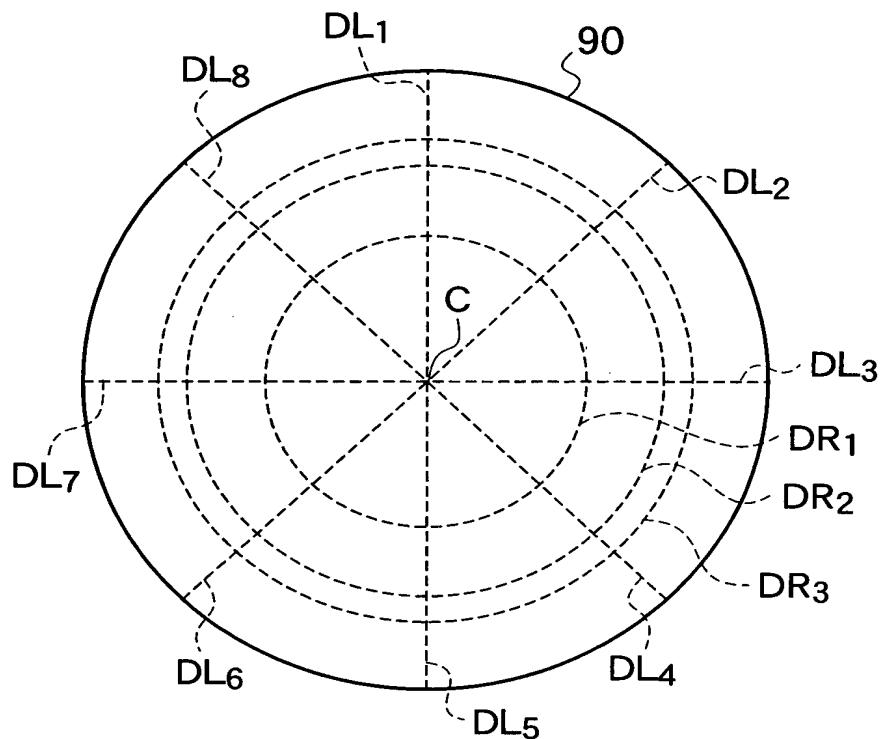
FIG. 6

PRODUCT B WAFER NUMBER	ELECTRIC TEST RESULT
5	 <p>100e 94a 94b</p>
6	 <p>100f 94a 94e</p>
7	 <p>100g 94a 94d</p>
8	 <p>100h 94a 94c 94e</p>
9	 <p>100i 94a 94e</p>

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FIG. 7

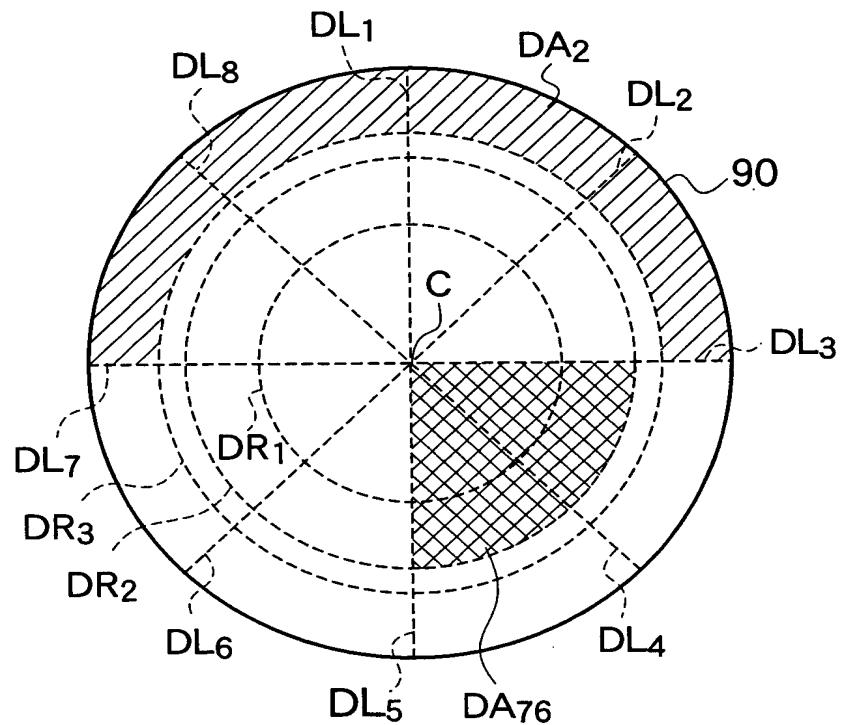
PRODUCT C	ELECTRIC TEST RESULT
WAFER NUMBER	
10	
11	
12	
13	

**FIG. 8****FIG. 9**

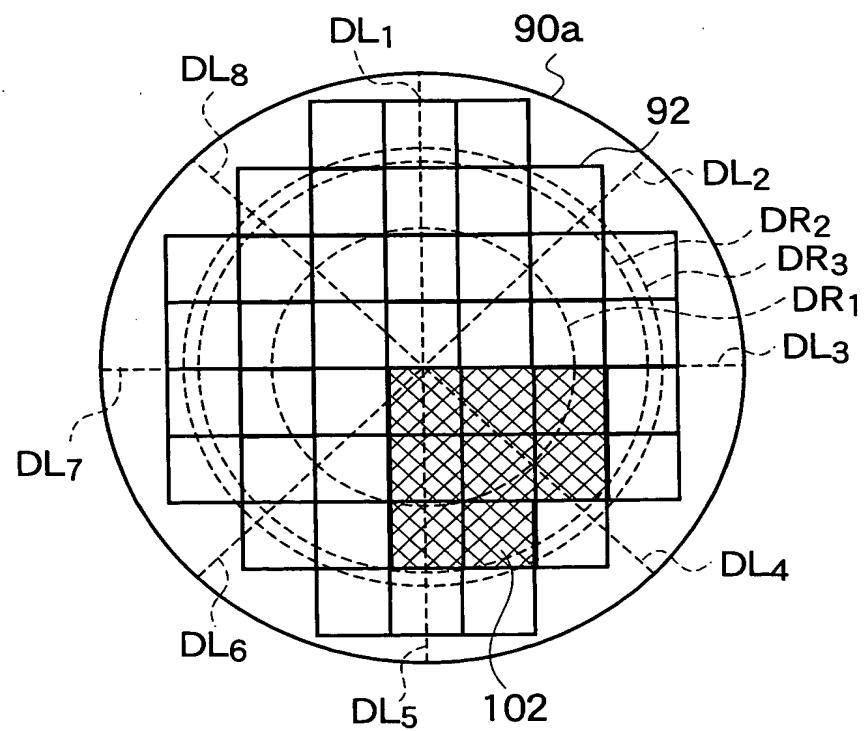
AREA NUMBER	SUBAREA
1	$[ DR_3 OUTSIDE ] \vee [ DL_3 - DL_4 - DL_5 - DL_6 - DL_7 ]$
2	$[ DR_3 OUTSIDE ] \vee [ DL_7 - DL_8 - DL_1 - DL_2 - DL_3 ]$
3	$[ DR_2 OUTSIDE ] \vee [ DL_8 - DL_1 - DL_2 - DL_3 - DL_4 ]$
...	...
76	$[ DR_2 INSIDE ] \vee [ DL_3 - DL_4 - DL_5 ]$
...	...
150	$[ DR_1 INSIDE ] \vee [ DL_4 - DL_5 - DL_6 - DL_7 - DL_8 ]$

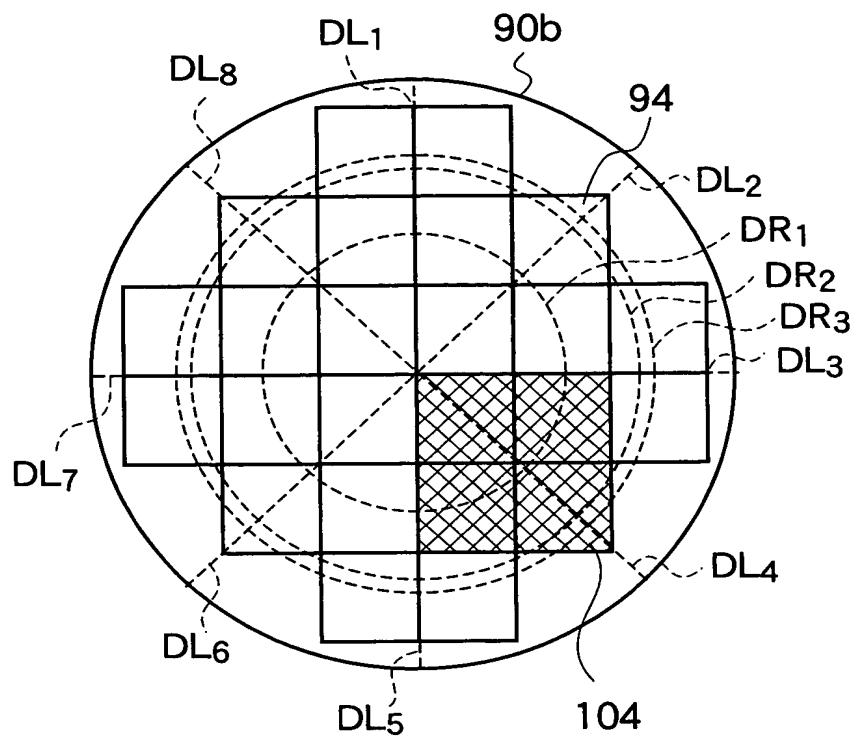
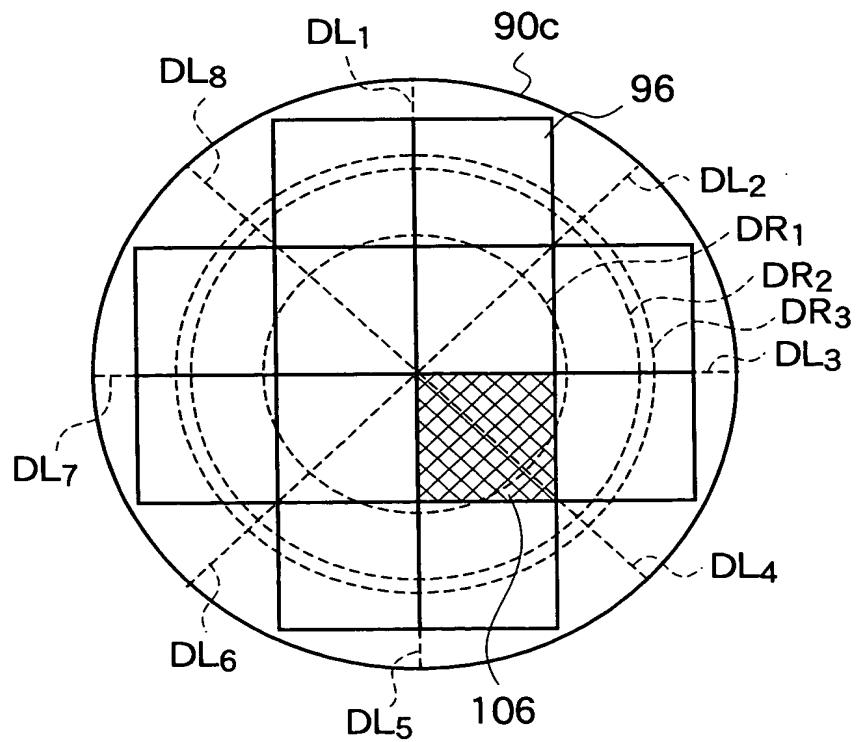
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**FIG. 10**



**FIG. 11**



**FIG. 12****FIG. 13**

**FIG. 14**

PRODUCT A		WAFER NUMBER			
ELECTRIC TEST	AREA NUMBER	1	2	3	4
DC	1	0.3	0	0.01	0.32
	2	0.5	0	0	0.12
	3	0.2	0.01	0	0.05
	150	0.5	0	0	0.32
FUNCTION	1	0	0.67	0	0
	2	0	0.23	0.02	0
	3	0.01	0.15	0	0.01
	150	0	0.42	0	0
MARGIN	1	0	0	0.2	0.01
	2	0	0.01	0.1	0
	3	0	0	0.03	0
	150	0.02	0	0.12	0

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FIG. 15

ANALOGOUS ELECTRIC TEST	PRODUCT A , WAFER No.1			PRODUCT B , WAFER No.5		
	ELECTRIC TEST	AREA NUMBER	FAILURE DENSITY	ELECTRIC TEST	AREA NUMBER	FAILURE DENSITY
ANALOGOUS ELECTRIC TEST 1	DC FAILURE	1	0.3	POWER SHORT FAILURE	1	0.28
		2	0.5		2	0.43
		3	0.2		3	0.1
		:	:		:	:
		150	0.5		150	0.67
ANALOGOUS ELECTRIC TEST 2	FUNCTION FAILURE	1	0	FUNCTION FAILURE + OTHER LOGIC FAILURE	1	0
		2	0		2	0.01
		3	0.01		3	0
		:	:		:	:
		150	0		150	0
ANALOGOUS ELECTRIC TEST 3	MARGIN FAILURE	1	0	FREQUENCY FAILURE	1	0
		2	0		2	0.01
		3	0		3	0
		:	:		:	:
		150	0.02		150	0

FIG. 16

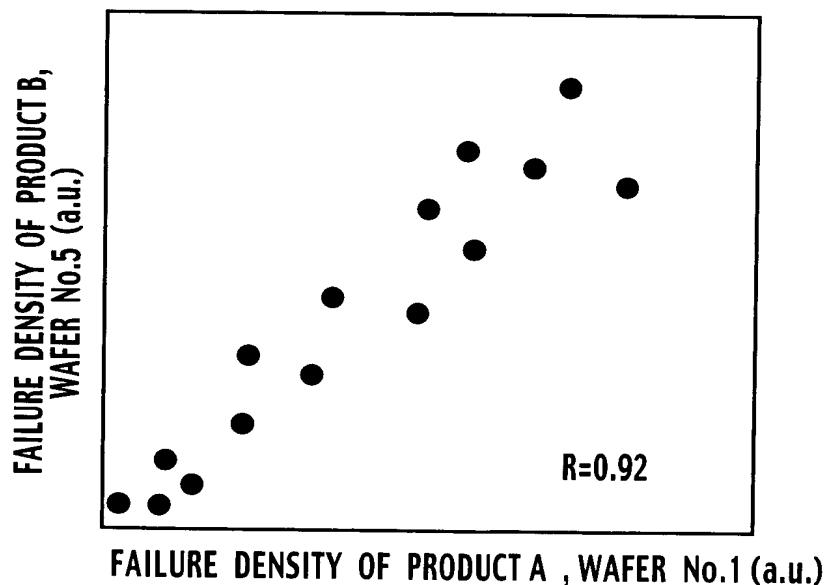
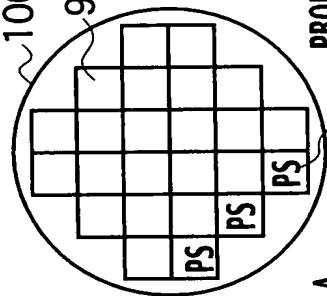
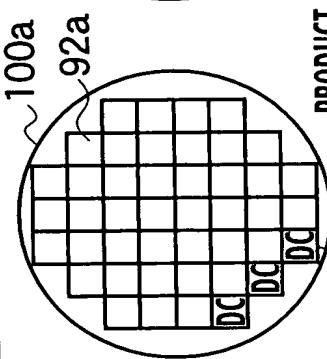
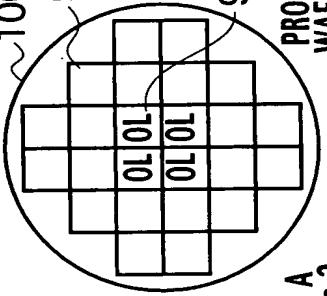
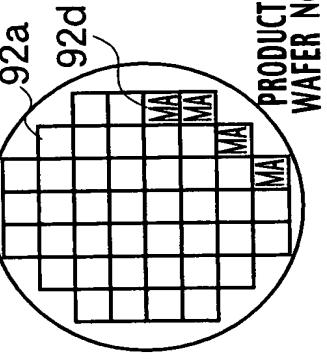
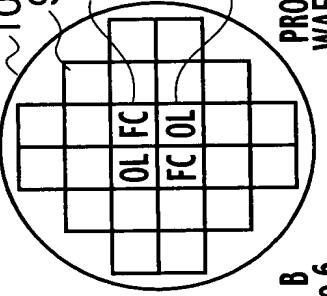
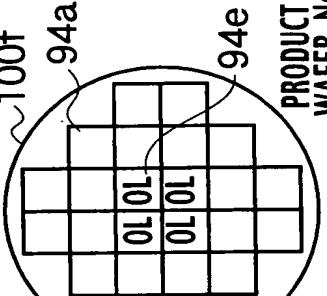
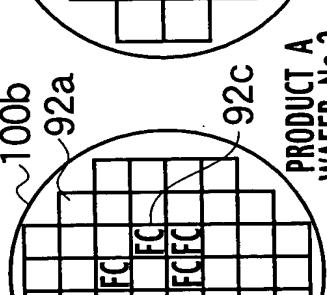
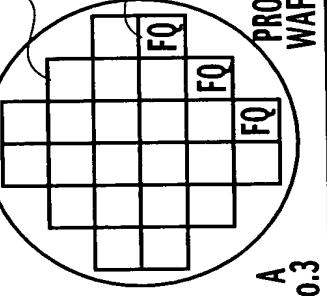
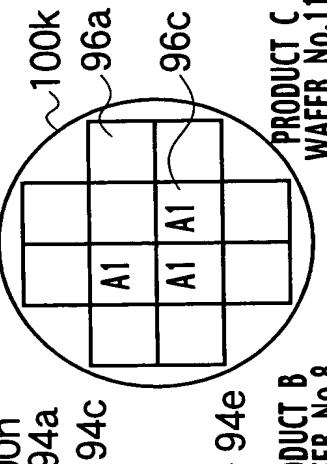
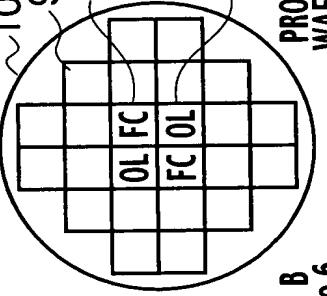
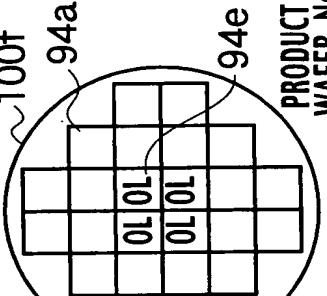
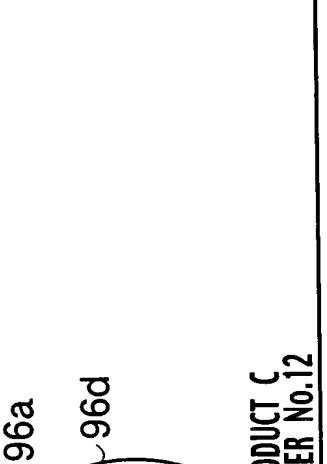
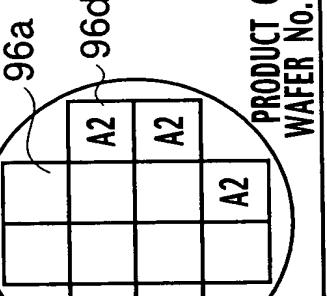
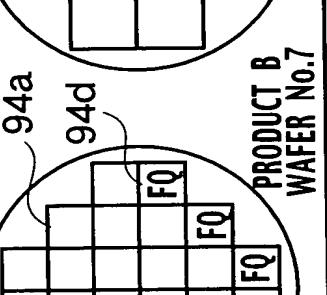
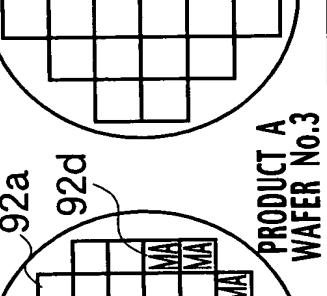
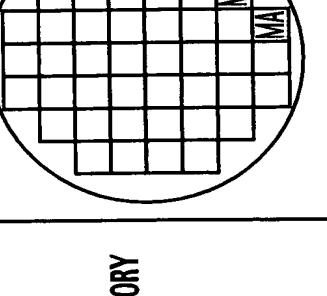
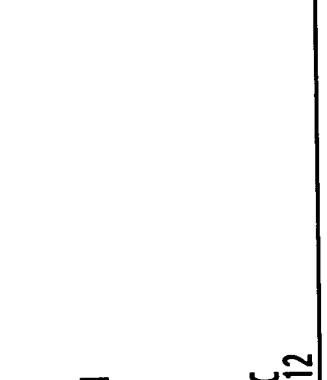
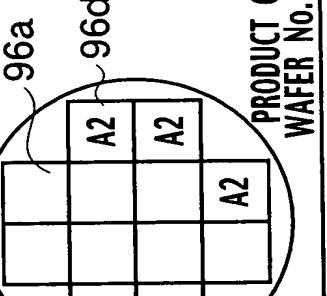
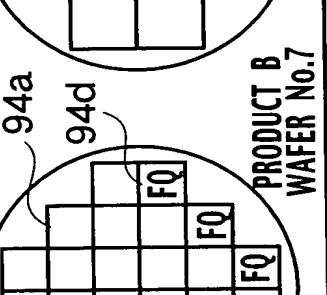
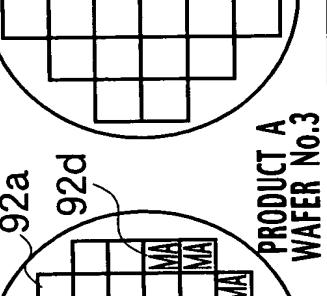
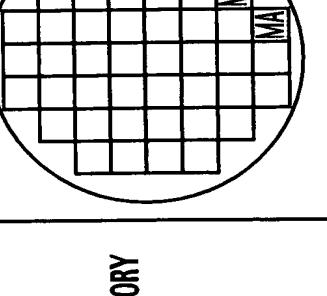


FIG. 17

		PRODUCT A		PRODUCT B		PRODUCT C	
		WAFFER No.1	WAFFER No.2	WAFFER No.3	WAFFER No.4	WAFFER No.5	WAFFER No.10
PRODUCT A	WAFFER No.1	1	0.01	0.12	0.08	0.92	0.91
PRODUCT A	WAFFER No.2	0.01	1	0.03	0.09	0.08	0.01
PRODUCT A	WAFFER No.3	0.12	0.03	1	0.12	0.01	0.09
PRODUCT A	WAFFER No.4	0.08	0.09	0.12	1	0.23	0.01
PRODUCT B	WAFFER No.5	0.92	0.08	0.01	0.23	1	0.87
.....							
PRODUCT C	WAFFER No.10	0.91	0.01	0.09	0.01	0.87	0.07
.....							
PRODUCT C	WAFFER No.13	0.01	0.01	0.01	0.02	0.09	0.07
.....							
							1

**FIG. 18**

CATEGORY 1	CATEGORY 2	CATEGORY 3
    <p>PRODUCT A WAFER No.1</p> <p>100a ~92a</p> <p>100e ~94b</p> <p>96a ~100j</p> <p>92b ~92b</p>	        <p>PRODUCT B WAFER No.5</p> <p>100b ~92a</p> <p>92c ~92c</p> <p>100f ~94a</p> <p>94a ~94b</p> <p>94c ~94c</p> <p>94d ~94d</p> <p>94e ~94e</p> <p>100h ~94e</p>	         <p>PRODUCT C WAFER No.10</p> <p>100i ~96a</p> <p>96a ~100k</p> <p>96c ~96c</p> <p>96d ~96d</p> <p>96e ~96e</p> <p>96f ~96f</p> <p>96g ~96g</p> <p>96h ~96h</p> <p>96i ~96i</p> <p>100l ~96i</p> <p>PRODUCT B WAFER No.6</p> <p>PRODUCT C WAFER No.11</p> <p>PRODUCT B WAFER No.7</p> <p>PRODUCT A WAFER No.3</p>

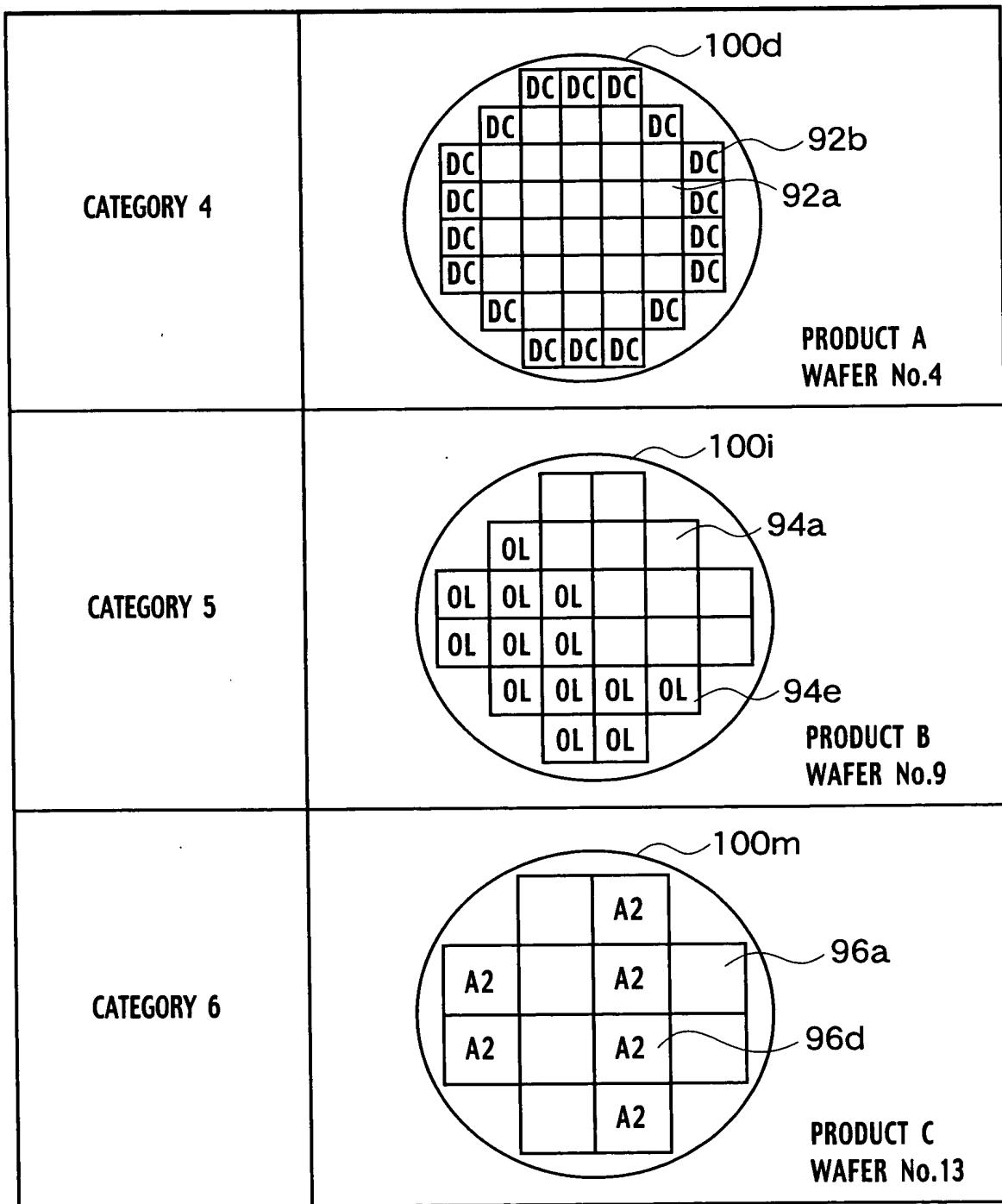
**FIG. 19**

FIG. 20

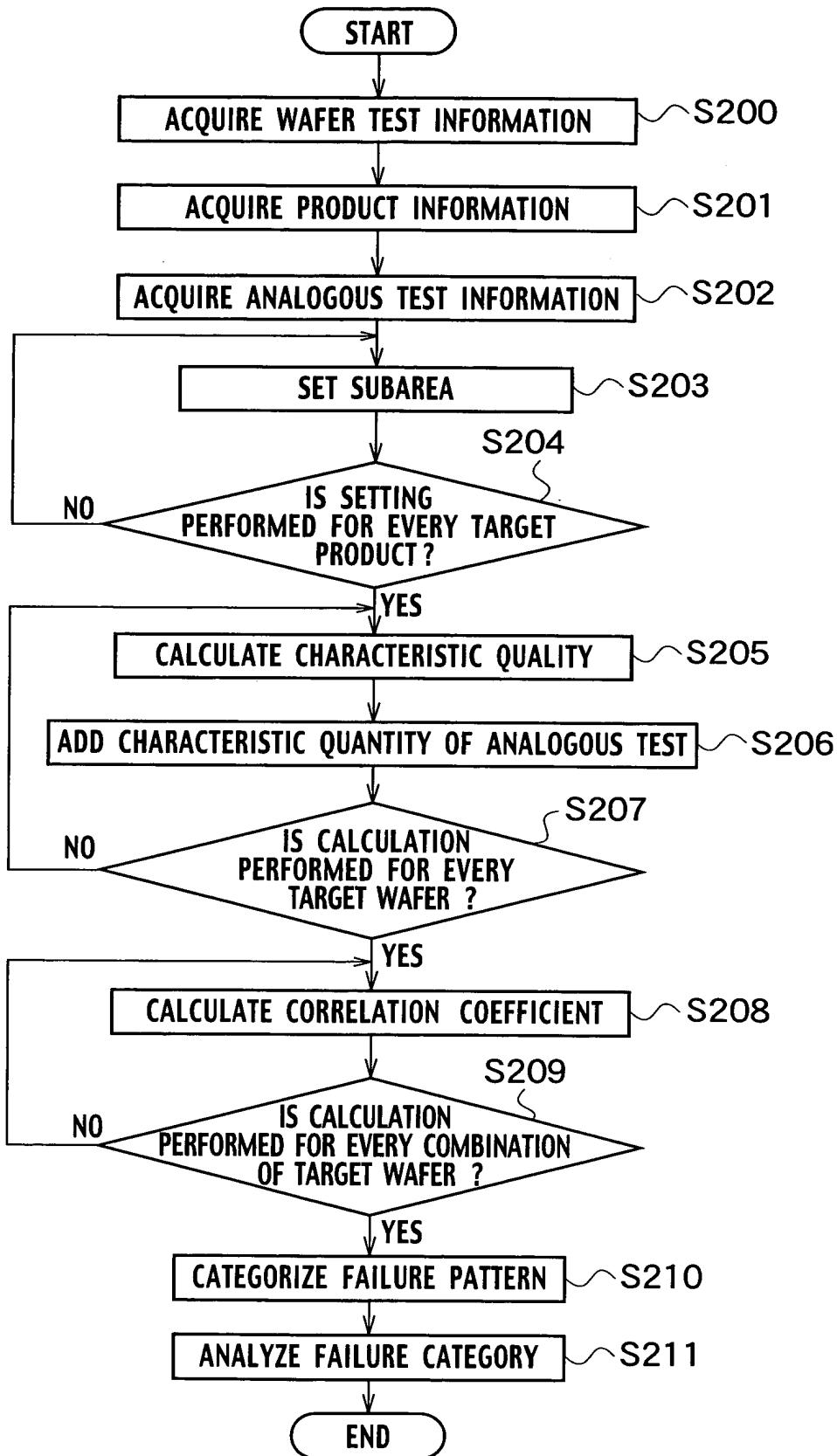


FIG. 21

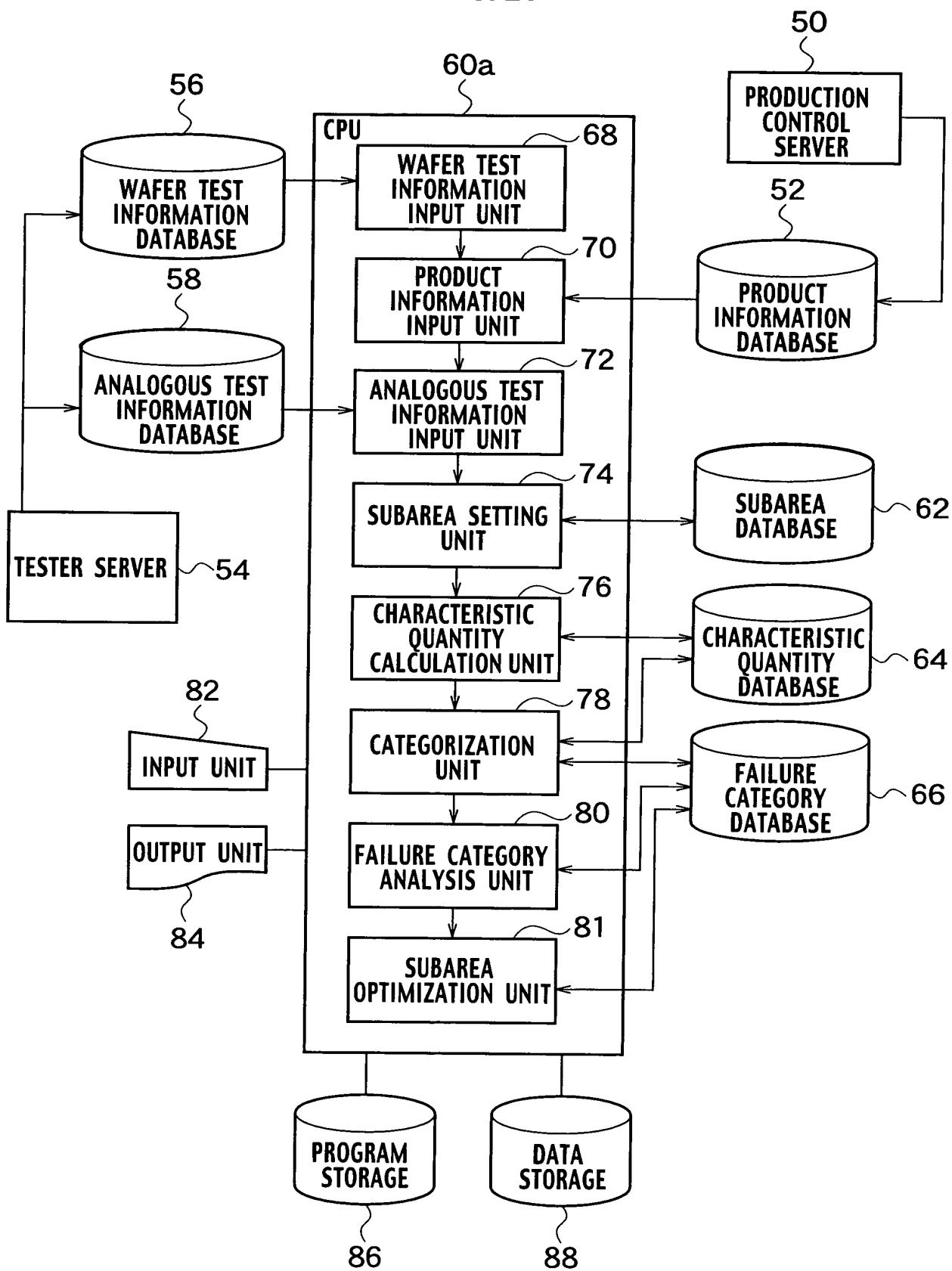
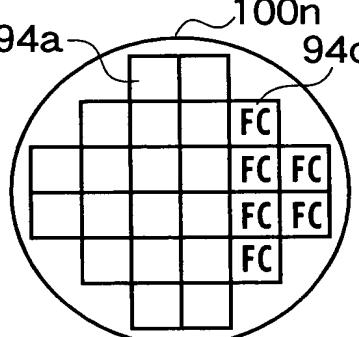
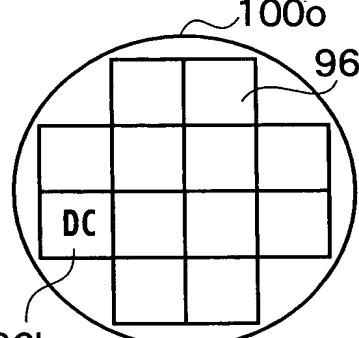


FIG. 22

	PASS / FAIL MAP	ABNORMAL PROCESS NUMBER	ABNORMAL MANUFACTURING APPARATUS	TEST STATISTIC
CATEGORY 7	 <p>94a 100n 94c</p> <p>FC FC FC FC FC FC</p>	136	M1	13.6
CATEGORY 8	 <p>100o 96a</p> <p>DC</p>	96	P1	12.7

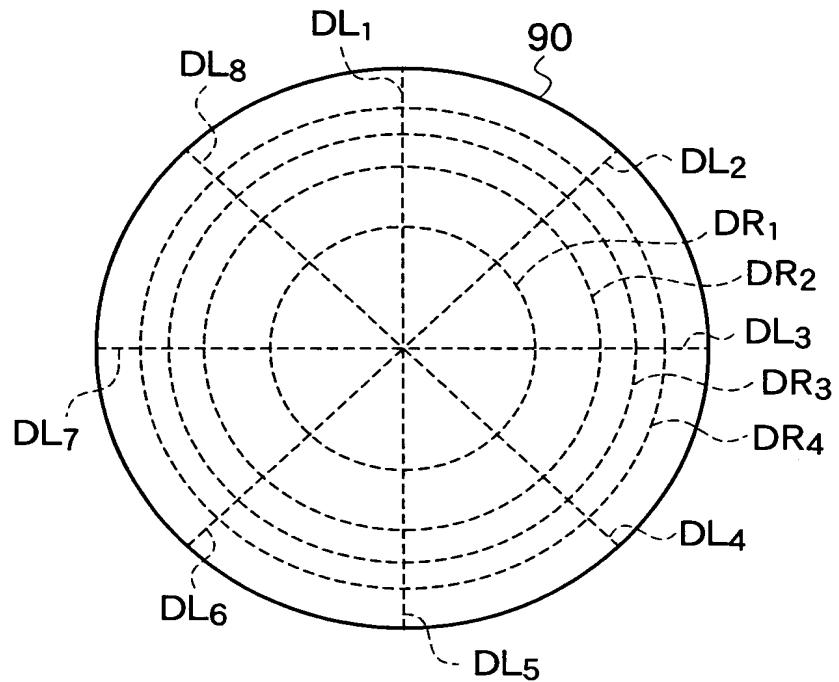
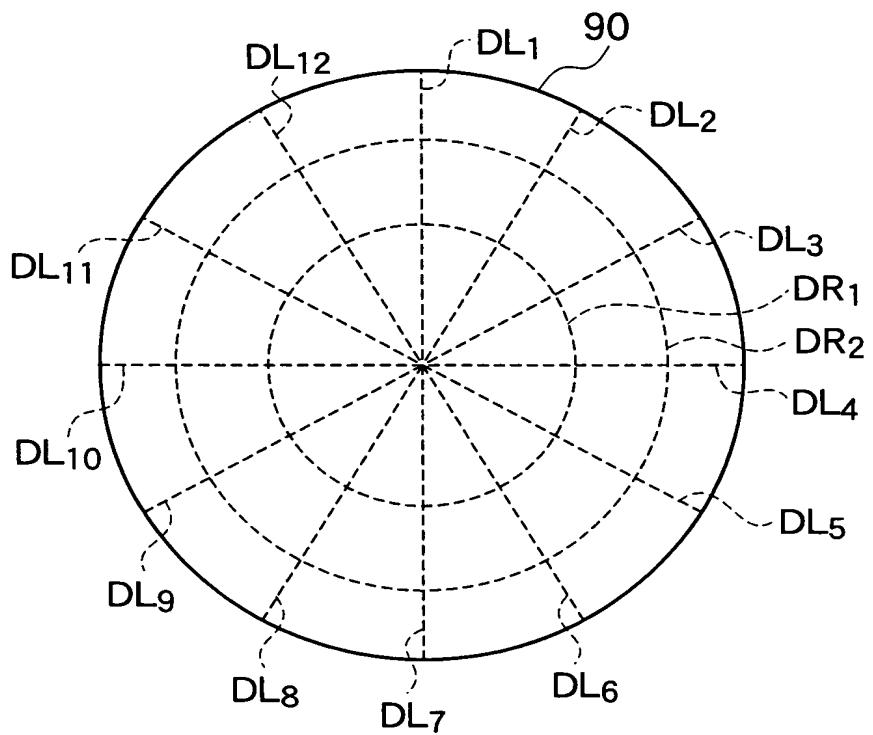
**FIG. 23****FIG. 24**

FIG. 25

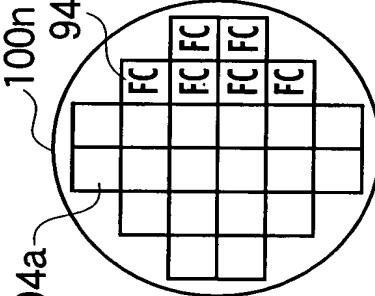
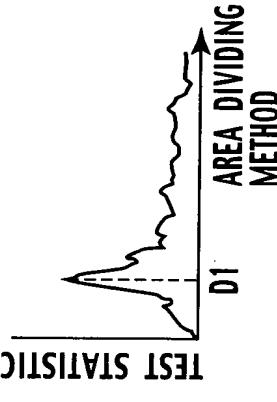
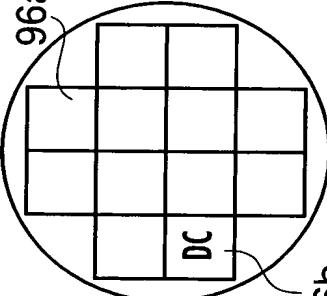
PASS / FAIL MAP	VARIATION OF TEST STATISTIC	ABNORMAL PROCESS NUMBER	ABNORMAL MANUFACTURING APPARATUS	TEST STATISTIC
94a	 <p>100n 94c</p> <p>CATEGORY 7</p>	 <p>D1 : DIVIDING CIRCLE:2 DIVIDING LINE:5</p>	<p>136</p> <p>M1</p>	<p>27.6</p>
96b	 <p>100o 96a</p> <p>CATEGORY 8</p>	 <p>D2 : DIVIDING CIRCLE:6 DIVIDING LINE:12</p>	<p>82</p> <p>P2</p>	<p>24.3</p>

FIG. 26

